FIGURE 1

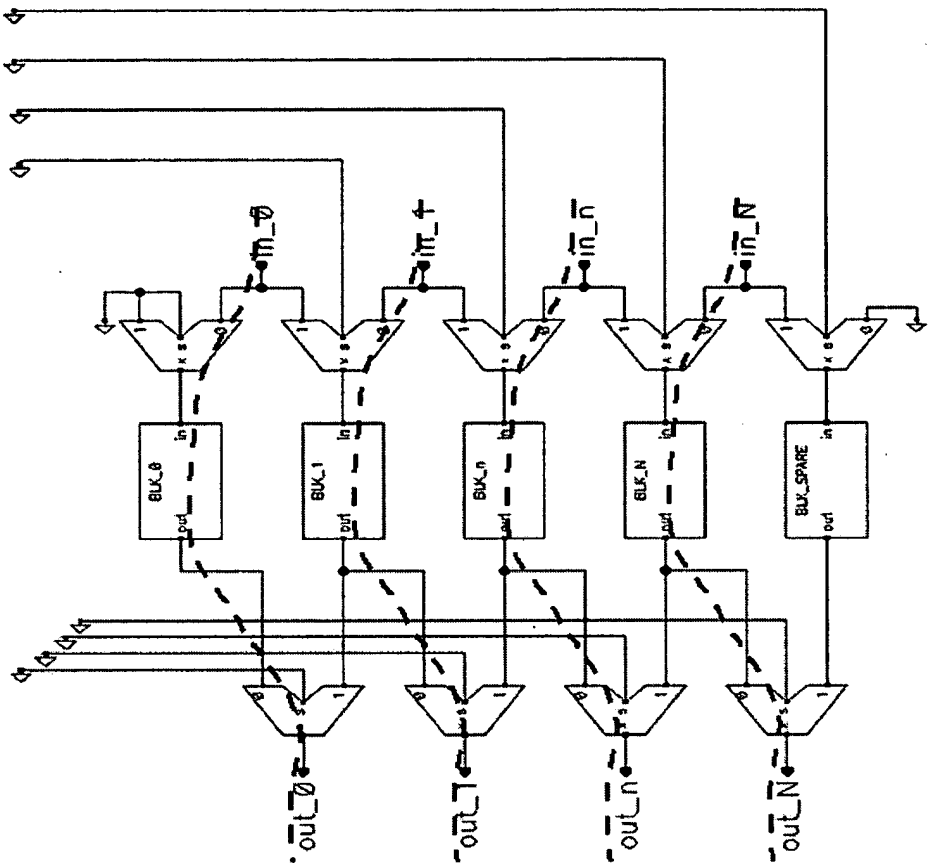

in_0
in_1
in_n
in_N
BLK_0
BLK_1
BLK_n
BLK_N
BLK_SPARE
out_0
out_1
out_n
out_N

FIGURE 2

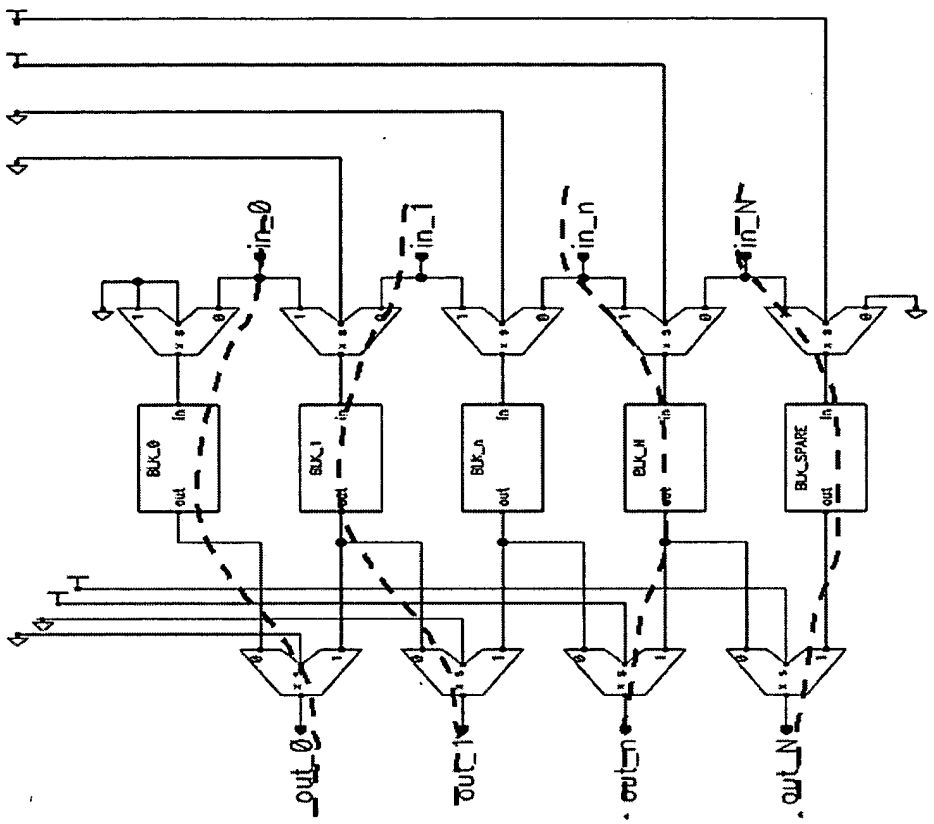

in_0
in_1
in_n
in_N
BUK_0
BUK_1
BUK_n
BUK_N
BUK_SPARE
out_0
out_1
out_n
out_N

FIGURE 3

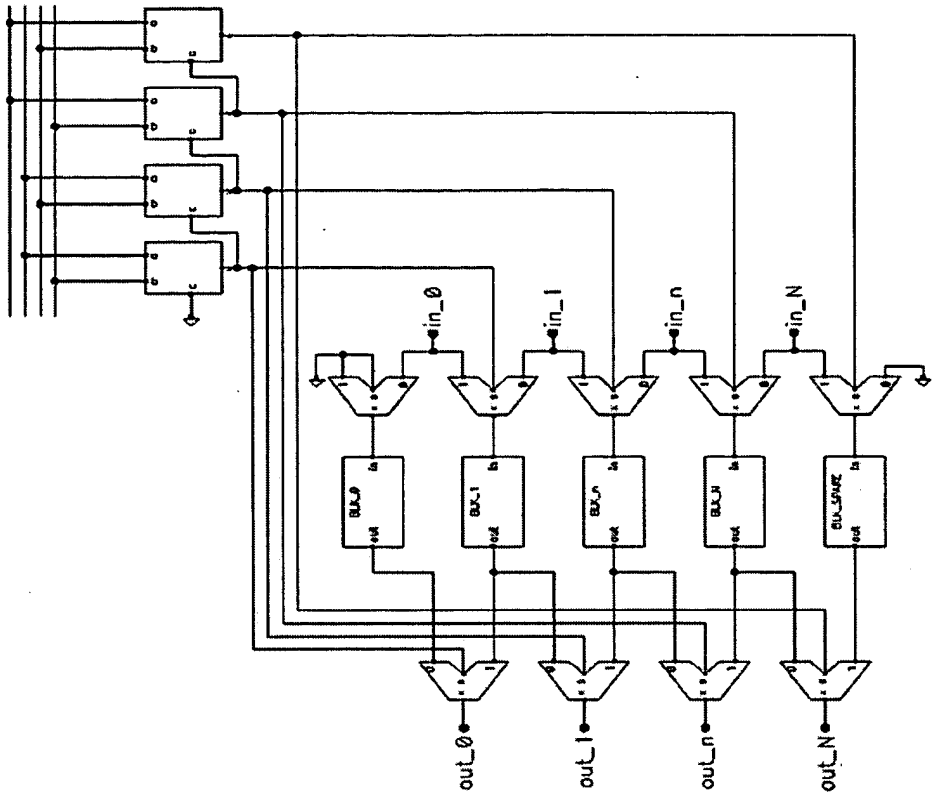


FIGURE 4

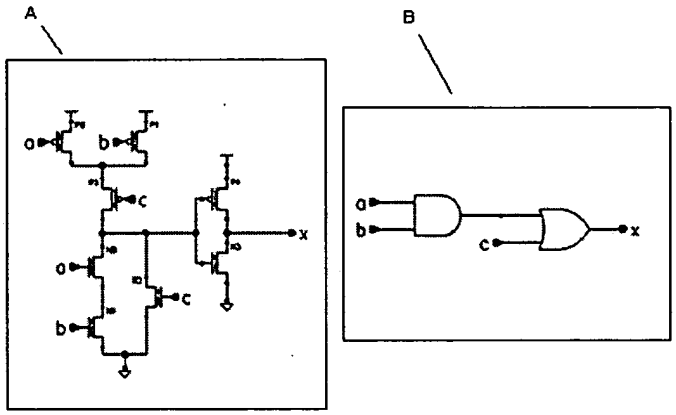
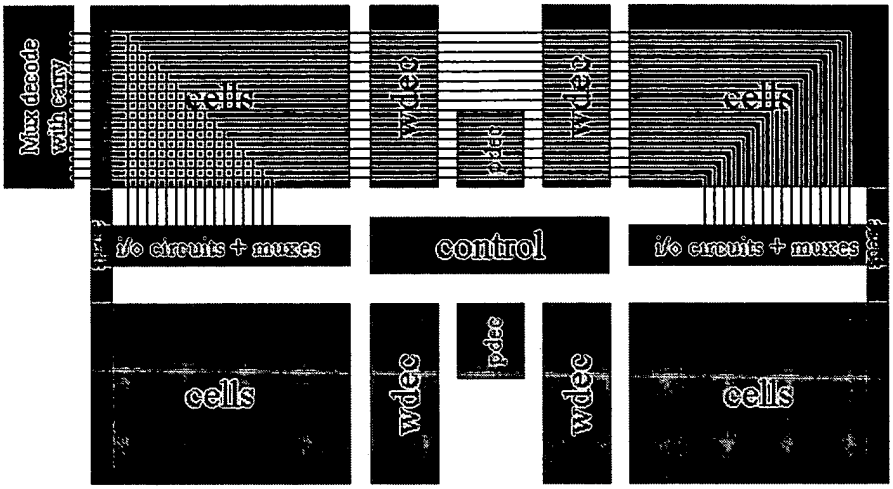


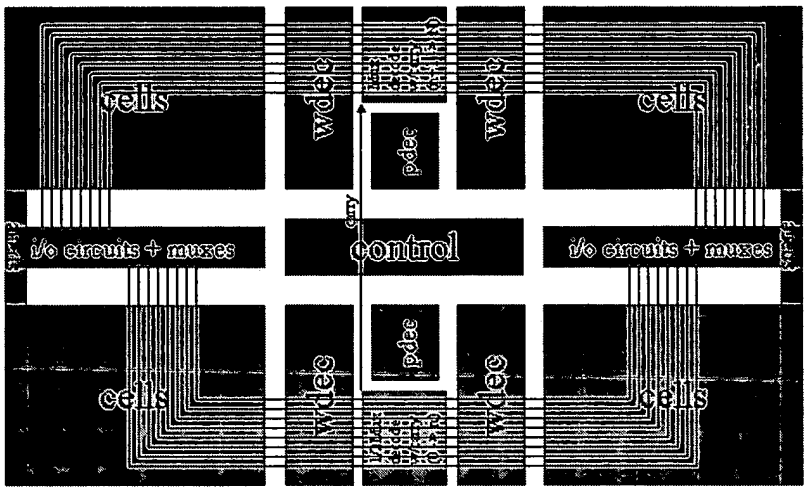
FIGURE 5



Mux decode requires extra space

One vertical wire (blockage) per i/o circuit

FIGURE 6



Mux decode fits in whitespace

One vertical wire (blockage) per i/o circuit

FIGURE 7

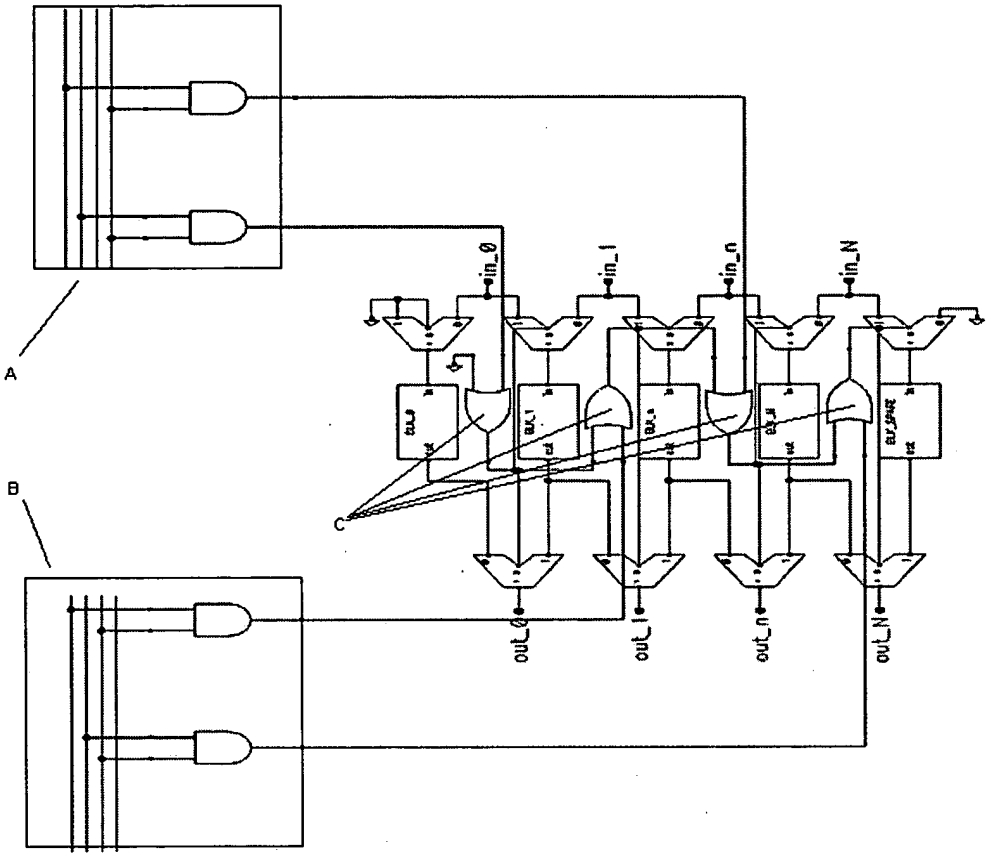
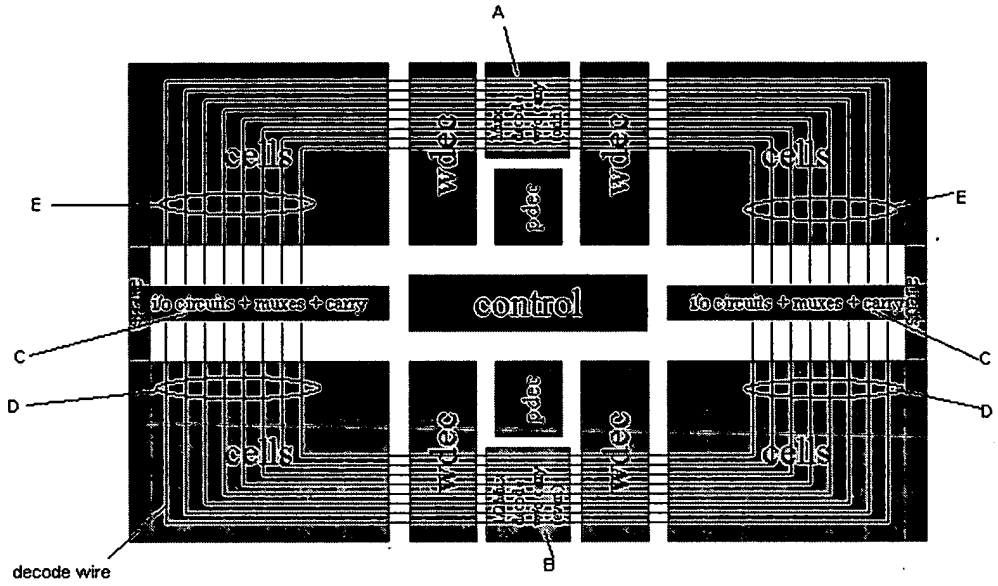


FIGURE 8



Mux decode fits in whitespace

One vertical wire (blockage) per **pair** of i/o circuits (1/2 the vertical blockages)